

SCEPTRE: SoC Multiprocessor Partitioning Optimization, Modeling, and Compilation

Background

Digital technologies have sparked a new dynamic on the consumer market by promoting the **emergence of a plethora of innovative new applications that combine communication and multimedia processing capabilities on a single chip.**

As a result, the number of transistors on a single chip (currently tens of millions) and the size of embedded software (hundreds of thousands of lines) have continued to grow. One of the main challenges System-on-Chip (SoC) developers must face is how to reach the **best possible compromise between the hardware/software partitioning of the different functions of the circuit in order to optimize product cost, performance, and flexibility while working within real-time limitations.**

Partners

Corporate

STMicroelectronics

SME

CapsEntreprise

Research laboratories

ENSL - INRIA Rhône-Alpes - INRIA Rennes INP G - TIMA - UJF - Verimag

Key figures

Budget: €9.3 million

Duration: 3 years

Human resources allocated: 65 people per year

Innovation

Hardware- and software-based solutions traditionally present a number of problems—most notably slower execution speeds for software and a lack of flexibility for hardware. In order to overcome these problems and speed up the hybrid-system development cycle, this project aims to combine in a new way two well-known fields:

- Multiprocessor systems
- Reconfigurable processors

The project will also take in to account constraints such as cost, energy-consumption, performance, and time-to-market.

More specifically, the purpose of the project is **to develop a set of tools** (debugging system, software on processor distribution, detection of hardware extensions, etc.) **and an associated platform to facilitate the implementation of multimedia algorithms and the generation of optimized code over a multiprocessor network of reconfigurable processors.**

