DAC 2017 MINALOGIC SHOWCASE

DAC 2017 | Austin, TX | June 18-22

SPOTLIGHT ON THE EDA INNOVATORS IN FRANCE

La Région Auvergne-Rhône-Alpes

AEPI Invest in Grenoble-Isère, France www.grenoble-isere.com

MINALOGIC

leti CEA tech

MINALOGIC

54 DESIGN AUTOMATION CONFERENCE

La FRENCH TECH

Minalogic is the global innovation cluster for digital technologies, serving France's Auvergne-Rhône-Alpes region, with its main office in Grenoble, France.

FOREWORD

Minalogic supports its members by fostering collaborative R&D in Micro- and Electronics, Photonics and Software, and nurturing its member companies with business coaching services throughout all phases of their growth.

CEA Leti, Cadence, HP, Mentor Graphics, Schneider Electric, Silvaco, SOITEC, STMicroelectronics and Synopsys-Atrenta are among the worldwide leaders and innovators who have significant R&D activities located in Grenoble, benefiting from its unique collaborative culture, mixing research, academia, start-ups and large groups.

Therefore, it should come as no surprise that among its 350 member companies, Minalogic and its Grenoble-based ecosystem have nurtured more than 20 EDA start-ups over the past 10 years.

These EDA start-ups cover the entire SOC and System design spectrum, from system specifications to RTL design, physical design and mask processing, targeting all electronic products: digital, analog, RF, mixed signal, at board- and chip-level. Of course, the EDA market is global, and therefore, most of these EDA start-ups have offices in the USA and in Asia.

Over the years, established EDA vendors have grown their R&D teams in Grenoble and throughout France, as well, both organically and through acquisitions.

Nestled at the foot of the gorgeous mountains of the French Alps in Grenoble, these companies and other members from other French tech hubs, operate within a world-class R&D ecosystem, benefiting from a pool of engineering and PhD talent among the most recognized in the world, the proximity of SoC and system product design activities, silicon R&D (CEA-LETI , SOITEC, ST) and silicon manufacturing (ST). At LETI for instance, joint R&D labs with EDA companies enable immediate access to state-of-the-art silicon and SoC data, drastically reducing the feedback loop between EDA tools and their application on actual silicon. FD-SOI and RF-SOI are among the key silicon technologies born in Grenoble in recent years.

At DAC 2017, Minalogic is pleased to showcase this best-kept secret: the EDA start-ups which benefit from the unfair advantage of being born in the innovation ecosystem of France and... did I mention they live in the French Alps? ☺

Philippe MAGARSHACK
President of Minalogic

Visitor

ASELTA

ASELTA operates in the IC manufacturing world and provides software solutions for wafer and mask patterning, optimizing the use of e-Beam/multibeam lithography equipment for sub-20nm nodes. Aselta Inscale is a complete, all-in-one solution, with a unique model based correction technology (on a full e-beam lithography process). It allows better lithography mask quality, increasing wafer yield. It enables next generation lithography related to EUV, ILT, Multibeam etc., necessary to cope with Moore's law.

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Visitor

ASYGN

ASYGN is a sensor electronics specialist. ASYGN serves the MEMS industry by delivering integrated circuits, lab instruments and software tools for the design, verification and characterization of complete sensor systems.
Recent releases from Asygn include the AS3125 chip for high-performance multi-DOF MEMS IMU, the dBox-Z1 instrument and AS3126 chip for high-frequency resonant sensor characterization, and Tactyle MX for the simulation and verification of Image sensors.

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CADENCE

Cadence enables electronic systems and semiconductor companies to create the innovative end products that are transforming the way people live, work and play. Cadence software, hardware and semiconductor IP are used by customers to deliver products to market faster. The company's System Design Enablement strategy helps customers develop differentiated products—from chips to boards to systems—in mobile, consumer, cloud datacenter, automotive, aerospace, IoT, industrial and other market segments. Cadence is listed as one of Fortune Magazine's 100 Best Companies to Work For.

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Booth 320

CMP (CIRCUITS MULTI-PROJETS)

CMP is a Multi-Project Wafer (MPW) service organization in ICs and MEMS for prototyping and low-volume production. CMP enables prototypes fabrication on industrial processes at very attractive costs and offers it great technical expertise in providing MPW and related services for Universities, Research Laboratories and Industrial companies' prototyping. Advanced industrial technologies are made available in CMOS, SiGe BiCMOS, HV-CMOS, SOI, MEMS, 3D-IC, mostly from STMicroelectronics and ams.

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Visitor

CWS (COUPLING WAVE SOLUTIONS)

CWS is a leader in solutions for interference analysis in complex chip designs incorporating RF and analog blocks. Our software bundle WaveIntegrity is used by chip architects and designers to drive the chip design floorplanning and by package and PCB designers to integrate the noise-related design constraints in the final chip operational environment. The SiPEX tool provides a unique solution to help foundries and fabless offer better RF device performances, and to deliver higher quality simulation models.

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Booth
1220

DEFACTO TECHNOLOGIES

Defacto Technologies is an innovative chip design software company providing breakthrough RTL platforms to enhance integration, verification and Signoff of IP cores and System on Chips. After more than 10 years of recognized leadership in Design for Test at RTL, Defacto is now offering a complete EDA solution to cover advanced Design Restructuring, Design Verification, Low-Power Design, IP Integration & RTL Signoff needs.

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DOLPHIN INTEGRATION

Dolphin Integration contributes to «enabling low-power Systems-on-Chip» for worldwide customers. Over 30 years of experience in the integration of silicon IP components, providing services for ASIC/SoC design and fabrication with its own EDA solutions, make Dolphin Integration a genuine one-stop shop addressing all customers' needs for specific requests. Dolphin Integration is the provider of innovative modeling and simulation EDA solutions.

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EVADERIS

eVaderis is the first company worldwide offering innovative IP solutions based on new disruptive embedded NVM: MRAM, ReRAM. eVaderis provides cost-effective and CMOS-compatible non-volatile products, ranging from single memory cuts and logic libraries to memory compilers and IoT-optimized subsystem processor hard macros. eVaderis products cover a wide range of markets and applications: (colon) wearables, mobile, infrastructures and IoT. For all of them, we can help the customer to analyze and overcome the multiple limitations of the current technologies (eSRAM, eFlash, CMOS registers and standard cells) and improve the final chip design.

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INTENTO

Intento-design (2015), operates in the Analog IC EDA market; it proposes an innovative design methodology for shortening the productivity gap inherent to the analog design process. Based on 25 years of research, the Intento solution accelerates the design of analog functions, helping the designer to automate the path from electrical behavior to transistor sizing. It allows fast technology migration and makes analog functions easily reusable.

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IROC TECHNOLOGIES

IROC Technologies provides the semiconductor industry with reliability analysis and management technical tools, test services, expert advisors and auditing. IROC's EDA tools, TFIT and SOCFIT, enable foundries, IP designers and component suppliers to develop high-reliability solutions for automotive, avionics, telecommunications and medical devices. IROC's test services provide fast and accurate methods of SER test and analysis. Lastly, the new reliability assessment services from IROC help automotive and aeronautical reliability engineers to perform ISO 26262 and DO 254 assessment of their hardware designs.

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Booth 1830

LETI-CEA TECH

Leti is a technology research institute at CEA Tech and a key player worldwide in technologies combining miniaturization, high performance and low power. With a staff of 1,900 and a portfolio of 2,800 patents, Leti partners with global manufacturers, SMEs and startups to tailor innovative solutions that strengthen their competitive positions.
At Leti, Electronic Design Automation (EDA) is covered through common labs with CAD companies. These labs allow CAD companies to evaluate and enhance their tools using Leti advanced circuit and technology test cases.
Follow us: @CEA_Leti.

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Booth 2029

MAGILLEM

Magillem is a leading EDA software provider. Internationally renowned, we are present in 12 countries. 90% of our turnover is realized abroad.

Our innovative solution, introducing an XLM-based collaborative platform, supports our customers' R&D, from specification of their product to the documentation, and connects all business experts, especially in IoT and embedded systems' domain.

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Booth 1329

MENTA

Menta delivers standard-cell based, embedded FPGA IPs for SoC, ASIC and ASSP designs. Our technology lets you effortlessly update your silicon post-production, whether to fix a bug, implement customer-specific features, adapt to evolving standards, or enhance security. Menta IPs are delivered with standard EDA tools, and currently support process technologies including GLOBALFOUNDRIES (32SOI, 14LPP) and TSMC (28HPM, HPC+), among others.

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Booth 947

MENTOR GRAPHICS

Mentor Graphics Corporation, a Siemens business, is a world leader in electronic hardware and software design solutions, providing products, consulting services and award-winning support for the world's most successful electronics, semiconductor, and systems companies. Corporate headquarters are located at 8005 S.W. Boeckman Road, Wilsonville, Oregon 97070-7777.

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SCALINX

SCALINX is a fabless semiconductor company designing state-of-the-art Analog, Mixed-Signal & RF Integrated Circuits and Intellectual Property blocks for the Aerospace/Defense, Industrial and Communications markets. Our core business is to provide tailored solutions to OEMs and semiconductor companies developing high-end circuits and systems with ultra-low power requirements and reduced Bill of Material.

Our expertise spans from the sensor interface to the digital interface. SCALINX's IC design team has a cumulated expertise of more than 250 years in the semiconductor industry with a proven track record of first-time-right tape-outs that has led to many successful business stories.

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Booth
1447

SILVACO

Silvaco, Inc. is a leading IP and EDA provider of software tools used for process and device development and for analog/mixed-signal, power IC and memory design. The portfolio also includes tools for power integrity signoff, reduction of extracted netlist for simulation speed-up and variation analysis. Silvaco delivers a full TCAD-to-Signoff flow for displays, power electronics, radiation and advanced CMOS along with a complete production-proven IP portfolio including IP licensing and IP management solutions. Headquartered in Santa Clara, California, Silvaco has a global presence with offices in North America, Europe, and Asia.

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TIEMPO SECURE

TIEMPO SECURE develops and industrializes components for secure communicating devices (banking smartcards, ID documents, IoT connected objects). These components, available as IP cores, include a microcontroller and crypto-processors designed in a proprietary clockless technology, offering, therefore, a very high level of security against attacks and outstanding performance in speed/energy for contactless operations. TIEMPO also offers a synthesis tool for clockless designs.

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TIMA

The research activities of the TIMA Laboratory focus on the definition of EDA methods and tools for correct and efficient design, simulation, high-level synthesis, validation and test of digital integrated components and systems on chip. Its main strengths are fast and accurate simulation and synthesis of hardware/software integrated multiprocessors, correct design at the RT level, and validation and test at the system level.

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Booth 1729

XYALIS

Shrinking geometries, new manufacturing paradigms, exploding file sizes… It's time to rethink everything!

XYALIS phases in a new generation of tools redesigned to address the challenges of today's most advanced processes, with a focus on speed and memory usage.

From CMP fill, with GOTstyle, to Mask Data Preparation with automated frame generation, MPW placement and mask set edition, to layout manipulation, XYALIS' redeveloped engines leverage the power of a native OASIS.MASK internal representation.

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Minalogic is a global innovation cluster for digital technologies serving France's Auvergne-Rhône-Alpes region. The cluster supports the region's leading innovators by facilitating networking, fostering collaborative R&D, and providing companies with personalized assistance throughout all phases of business growth. The products and services developed by our members address all industries, from ICT and healthcare to energy and advanced manufacturing.

TARGET MARKETS :

- ICT
- Healthcare
- Energy
- Construction
- Advanced Manufacturing
- Transportation
- Sports & Outdoors

Minalogic was founded in 2005 and today boasts more than 350 members, including 300 companies. The cluster has certified nearly 519 projects that have secured total government funding of €836 million of the €2.1 billion in total R&D spending these projects represent. The 67 projects completed to date have resulted in 56 products (either on the market or in the process of being prepared for market release) and generated €1.58 billion in revenue.

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INVEST IN GRENOBLE-ISÈRE FRANCE

AEPI partners with Minalogic, CEA Leti and others to promote the Grenoble-Alps ecosystem and attract companies to southeastern France.

AEPI is based in Grenoble, one of the world's top microelectronics clusters, very well known in the EDA community.

With a North American office in California, AEPI offers information, contacts and services, all of which are complimentary and can be provided in confidentiality, to businesses exploring options in the area.

Many US companies active in EDA have operations and/or partnerships in the area. Over the years at DAC, an impressive percentage of exhibitors have been French companies, a majority of which have been Grenoble-based.

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COME AND MEET US AT

Tuesday, June 20, from 4-6 p.m. ROOM 8C, SECOND FLOOR MEZZANINE, Austin Convention Center

> Introduction speech by **Philippe Magarshack**, President of Minalogic & EVP, STMicroelectronics

> Remarks by Daniel Nenni de SemiWiki (Guest of Honor)

> Talks by

Eric Mottin, Microelectronics' Director – Minalogic
« Presentation of Minalogic & EDA Members & Specificities »

Firas Mohamed, General Manager – Silvaco France
« Fostering Innovation in TCAD, EDA & IP »

Thierry Collette, VP, Architecture, IC Design & Embedded Software Division, Leti
« Overview of Design & EDA Challenges for SOI Technology »

Ramy Iskander, CEO – Intento Design
« Accelerated Constraint-Driven Analog Design and Migration at Functional Level »

Isabelle Geday, CEO – Magillem
« Integrating Specification, Design and Documentation to Optimize SoC Design Cycle and Legacy Reuse »

Jean-Marc Talbot, Senior Engineering Director DSM/AMS – Mentor Graphics
Title TBD

> Networking reception

The event is free, **but please register in advance:**
http://www.grenoble-isere.com/dac/register.htm

MINALOGIC

AEPI Invest in Grenoble-Isère, France
www.grenoble-isere.com

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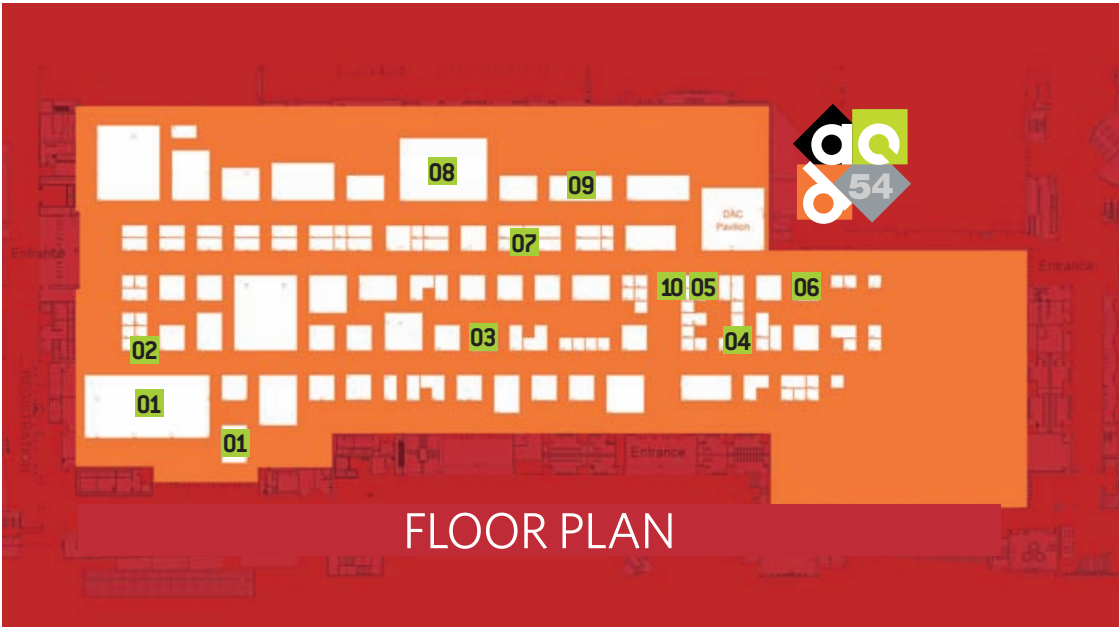

FLOOR PLAN

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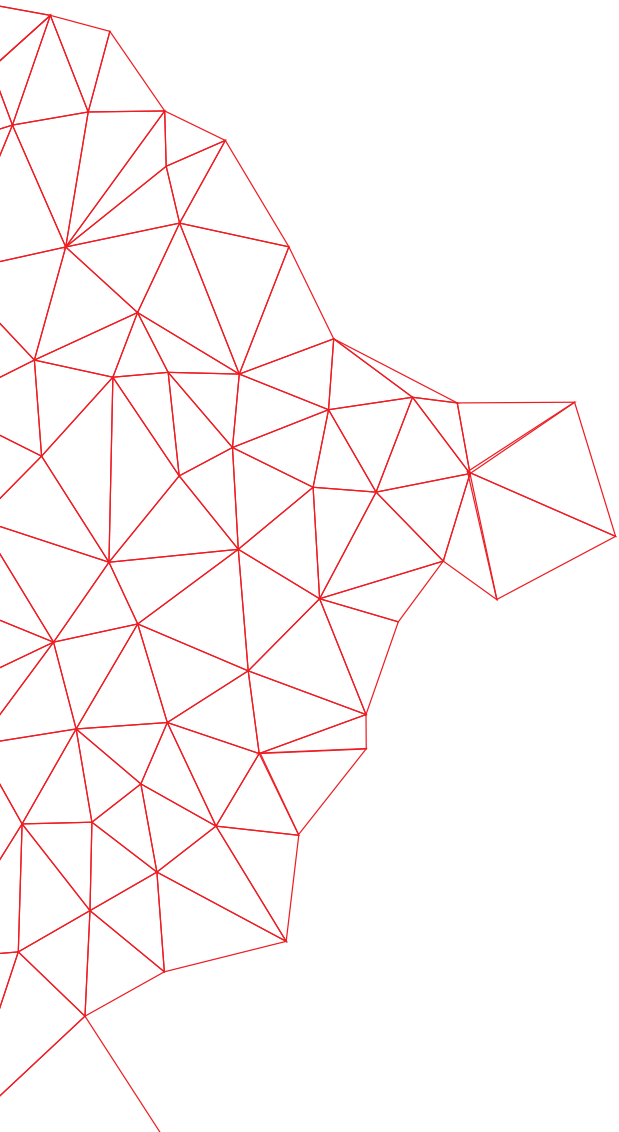


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