2018 CONFERENCE PROGRAM - EXHIBITION *English Speaking for all Presentations*

GENERAL CHAIR : J.L DIOT, NOVAPACK - TECHNICAL CHAIRS: M. GARNIER, ST MICROELECTRONICS & G. SIMON, CEA-LETI

TUESDAY MAY 15TH

Afternoon : 15h30 to 17h30	Lecture Karlheinz Bock (Institute for Electronic Packaging, TU Dresden Makalu Room) - Hetero-integration-Electronics packaging for multi-functional systems co-organized with IEEE-CPMT

WEDNESDAY MAY 16TH

8h45	Welcome to MINaPAD 2018	
9h00	Opening by Jean-Luc Diot (Auditorium)	
9h30	Keynote 1: Karlheinz Bock (T.U. Dresden): Electro-optical Hetero-integration (Auditorium)	
10h15	Exhibition Opening (Exhibition Hall)	
	Session A: Wafer Level Molding	**Session B: Joining**
10h45	Ultra-Low Warpage Epoxy Mold Compounds for Fan-Out Wafer Level Package Applications *(F. Duval, IMEC)*	Mechanical Behavior of Intermetallic in Cu-Sn Inter-Diffusion for Power Semi-Conductor Packaging *(Y. Bettahi, ST Microelectronics, Tours)*
11h10	Ultra-Low Warpage Liquid Encapsulation Technology for Advanced Wafer Level Packaging (WLP) *(R. Zhang, HENKEL Electronic Materials)*	A low Temperature Curing Hybrid Silver Sintering Die Attach Paste for High Reliability Power Semiconductor Applications *(S.Kanagavel, ALPHA Advanced Materials)*
16h25	5S-6S Wafer Level Encapsulation: Its Challenges and Solutions *(E. Kuah, ASM Technology)*	Innovative Adhesives for MEMS Packaging *(R. Kmeth, DELO Industrial Adhesives)*
	12h00/13h15 - Lunch (Exhibition Hall– Exhibition)	
13h15	Keynote 2: Erik Jung (IEM FRAUNHOFER): Advancement for Exponential Medicine driven by KET: Micro and Nanotechnology (Auditorium)	
	Session C: Embedded Components	**Session D: Fan In/Fan Out**
14h15	New Embedded Inductors for Power Converter Applications *(G. Weidinger, AT&S)*	High End Performance Application Key Driver for Advanced Packaging *(E. Jolivet, YOLE Développement)*
14h40	High Q 3D Inductors Embedded in a Silicon Interposer RF Platform *(G. Pares, CEA-LETI)*	Fan-in WLCSP Evolution, is Fan out Wafer Level an Extension of Fan-In or a New Platform? *(C. Zinck, ASE)*
	15h05/15h35 - Exhibition - Coffee Break sponsored by	
	Session E: Hi-Rel Packaging	**Session F: Advanced Process**
15h35	Multiphysics Design of Compact Photonic Devices *(A. Annoni, CORDON Electronics)*	20 µm Pitch Microbumps Assessment in Chip to Wafer Assembly Configuration *(A. Garnier, CEA-LETI)*
16h00	J. Lead Ceramic Packages for High Performance MEMS Accelerometers: Simulation and Experimental Results *(F-Y. Boillot, TRONIC'S Microsystems)*	Curved Sensors for Compact High-Resolution Wide Field Designs: Prototype Demonstration and Optical Characterization *(S. Caplet, CEA-LETI)*
16h25	Packaging Technologies for Harsh Environments Based on Silicon Carbide Substrates *(G. Spinola Durante, CSEM)*	Functional Glass Encapsulation for Micro-Systems *(M. Kuenzi, GLENCATEC)*
	Session G: Wafer Level Packaging	**Session H: Other Process**
16h50	Studies of the Electromigration Effect in RDL of Wafer-Level Fan-In and Fan-Out Packaging Using a Novel Analysis Approach *(A. Cardoso, AMKOR Portugal)*	A Brief Review of Die Bonding Technics *(G. Ribette, MICROTEST)*
17h15	Electrografted Seed Layer Deposition: An Advanced Metallization for Enhanced 12: 1 Aspect Ratio Mid-Process TSV *(C. Aumont, ST Microelectronics Crolles)*	Surface Preparation Using a Downstream Atmospheric Plasma, Application to Device Packaging *(G. Lecarpentier, (SETNA)*
17h40 -18h00	Exhibition	
19h30	Social Event Restaurant "L'Epicurien"	

THURSDAY MAY 17TH

8h30	Keynote 3: : Magali Vigier (AIRBUS) & Philippe Pons (AEROSPACE VALLEY Cluster): Advanced Electronics Boards in Avionics, PCB & Assembly, Challenges and Perspectives (Auditorium)	
	Session I: BGA Reliability	**Session J: Dicing/ Picking**
9h30	A New Experimental Methodology for Thermal Expansion Calculation and Its Applications for Package Warpage Prediction *(M. Rovitto, ST Microelectronics, Italy)*	Solutions for Thin and Tiny Dies with High Die Strength and for Thinning WL-CSP and e-WLB Wafers *(G. Klug, DISCO HI-TEC Europe GmbH)*
9h55	Innovative Experimental Setup for Creep Fatigue Interaction in Solder Joints Analysis *(S. Zanella, THALES Global Service)*	Key Properties for Successful Ultra-Thin Die Pick-up *(S. Behler, BESI Switzerland AG)*
10h20	Lead-free Solder Joints Robustness Improvement Using Bismuth Doping -Application to BGA *(L. Petit, ST Microelectronics Grenoble)*	Laser Based Full Cut Dicing Evaluations for Thin Si Wafers *(J. van Borkulo, ASMPT)*
	10h45/11h15 Exhibition - coffee break sponsored by	
	Session K: Flip-Chip Process & Applications	**Session L: Molded Packages**
11h15	New Flip-Chip Technology *(R. Windemuth, PANASONIC)*	nCapsulate, Added Value for (Sensor) System Assembly *(I. Van Dommelen, SENCIO)*
11h40	Direct Bonding with a New Flip-Chip Bonder for Production Environment *(P. Metzger, SET Corporation)*	Development of Cavity Power Packages Based on Liquid Crystal Polymer Thermoplastics *(J.L. Diot, NOVAPACK Technologies)*
12h05	Thermal Interface Materials Assembly and Reliability Challenge *(A. Taluy, ST Microelectronics Grenoble)*	New Generation of Routable QFN for Power SiP *(J. Abela, UTAC)*
	12h30/13h30 Lunch & Exhibition (Exhibition hall)	
	Session M: MEMS & SiP	
13h30	MEMS Technologies *(B. Boutaud, MISTIC)*	
13h55	MEMS and Sensor Packaging Evolution *(C. Zinck, ASE)*	
14h20	High Volume System-in-Package Manufacturing Using Traditional SMT Single in-line Solution *(W. Kwok, ASM Technology)*	
14h45-15h15	Exhibition/coffee break	
15h15	Keynote 4: Stéphane Bernabé (CEA-LETI): Key Challenges for Photonic Integrated Circuits Integration and Packaging (Auditorium)	
16h15	Best Paper Award	
16h30	End of MINAPAD 2018	

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Lecture: Hetero-Integration – Electronics Packaging for Multi-functional systems
(Karlheinz Bock, Institute for Electronics Packaging, TU Dresden, Germany)

Co-organized with IEEE-CPMT

The development of electronic packaging gains importance in the value chain of systems integration. Substrates, components and housing may not be solely manufactured before packaging but may be build-up during the packaging process itself. Such kind of hetero-integration strongly arguments to adapt systems packaging and device technologies from co-design towards co-manufacturing. Packaging develops towards a generic part of the systems concept and we may see much more process concepts needing to consider "packaging first".

Thin silicon chips, foil integration, 3D stacking of functional layers as well as 2.5 or 3D interposer enable such new system concepts. Co-integration of electrical and optical wave-guides is a consequence in order to cope with the increasing demand of bandwidth efficiency in communication systems. Additive manufacturing, 3D printing as well as self-assembly and self-alignment processes seems to be a possibility to complement with classic thin- and thick-film technologies and are needed to meet the requirements of systems in the near future.

Hetero-integration is of relevance for many system integration fields from functional electronic surface, power electronics modules, medical electronics, but, also for highly performant 3D integrated communication systems in the future for tactile internet and 5G mobile networks. This lecture introduces different aspects of hetero-integration at hand of technology examples.

KEY-NOTES MiNaPAD 2018

Key-note 1: Electro-Optical Hetero-Integration (Karlheinz Bock, Institute for Electronics Packaging, TU Dresden, Germany)

The development of electronic packaging gains importance in the value chain of systems integration. Substrates, components and housing may not be solely manufactured before the packaging process but may be build-up during the packaging process itself. Such kind of hetero-integration strongly arguments to adapt systems packaging and device technologies over the complete manufacturing process from co-design towards co-manufacturing.

This presentation focusses on the chances and challenges of packaging at hand of research examples aiming for: electrical and optical wave guide integration on interposer, mirror manufacturing for integrated optical wave guides, RF wave guide integration and combination with patch antenna as well as mm wave ICs embedding. Furthermore, in future, additive manufacturing, 3D printing as well as self-assembly and self-alignment processes will possibly complement with classic thin- and thick-film technologies and are needed to meet the performance, reliability, energy and cost requirements of 3D integrated high-performant electro-optical systems.

Key-note 2: Advancement for Exponential Medicine driven by KET: Micro and Nanotechnology (Erik Jung, IZM Fraunhofer, Germany)

Micro and nanotechnological advances have spurred a firework of innovations in the sector of medical diagnosis and therapy. Devices, which allow autonomously to monitor patient's progress, connected to a network of complementary sensors and decision-making systems and feeding this information back to assistive systems, will provide improved, highly individualized therapy, prevention and support for patients wellbeing. Stepping up the capabilities to work in the same dimension as the functional elements of the human body offers us now unprecedented opportunities to influence the biological processes down to the cellular level, with unforeseeable perspectives.

As of this, the key enabling technologies (KET), which have been developed in the past decade and continue in innovative applications, offer a critical mass for continuously fuelling the exponential growth of medical innovations. The talk will thus focus on the advancements seen in the integration of micro- and nanotechnology in the medical sector and their current and future use case perspectives.

Key-note 3: Advanced Electronic Boards in Avionics- PCB & Assembly Challenges and Perspectives (Magali Vigier, Airbus, France & Philippe Pons, Aerospace Valley cluster, France)

In a competitive context, avionics uses in the majority of cases COTS (commercial off-the-shelf) components and grasps opportunities for new functions, higher performance and integration with reduced cost, but shall adapt to technologies and components trends ruled by commercial - high volume & low-cost oriented applications and characterized by rapid changes.

The presentation will stress on:

- The avionics context highlighting the challenges and the main drivers;
- The embedded electronics requirements (reliability; life time...), 'green' directives & constraints (thermal, mechanical, EMC…);
- Examples of the current approach for assessing industrial maturity and reliability of PCB with highly integrated components;
- The overview of products roadmap, assembly technologies and new challenges.

Key-note 4: Key challenges for Photonic Integrated Circuits integration and Packaging (Stéphane Bernabé, CEA-Leti, France)

Circuit design in semiconductor like environments, laser integration and low-cost packaging remain key challenges for Silicon Photonics based modules.

They are addressed by developing dedicated design tools, novel laser integration strategies and by leveraging advanced packaging techniques. These developments are a mandatory step on the path to terabit class transceivers and photonic based computers.

MiNaPAD FORUM 2018

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May 16: **9h00 – 18h00**
May 17: **8h30 – 16h30**

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- **November 8th 2018**
  9th From Nano to Macro Powers Electronics and Packaging European workshop, Tours, France
- **February 2019 6 -7**
  14th ATW on Micropackaging and Thermal Management, La Rochelle, France

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MiNaPAD Forum 2018

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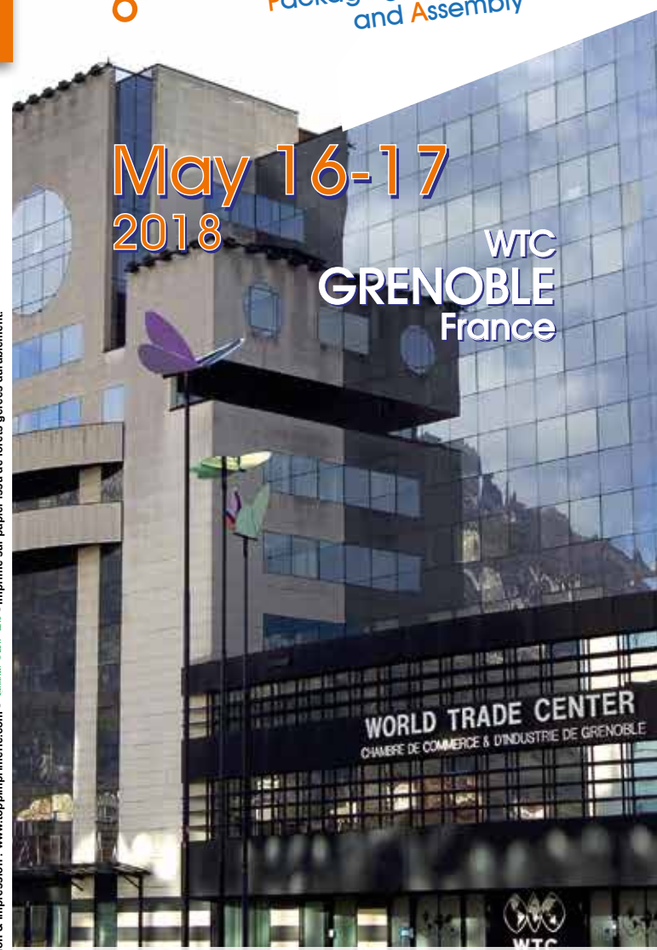

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