DAC 2016 MINALOGIC SHOWCASE

DAC 2016 | Austin, TX | June 5-9

SPOTLIGHT ON THE EDA INNOVATORS IN FRANCE









Minalogic is the global innovation cluster for digital technologies, serving France's Auvergne-Rhône-Alpes region, with its main office in Grenoble, France.

FOREWORD

inalogic supports its members by fostering collaborative R&D in Micro- and Nanotechnologies, Photonics and Software, and nurturing its member companies with business coaching services throughout all the phases of their growth.

CEA-LETI, Cadence, HP, Mentor Graphics, Schneider Electric, Silvaco, SOITEC, STMicroelectronics, and Synopsys-Atrenta are among the worldwide leaders and innovators who have significant R&D activities located in Grenoble, benefitting from its unique collaborative culture, mixing research, academia, start-ups and large groups.

Therefore, it should come as no surprise that among its 300 member companies, Minalogic and its Grenoble-based ecosystem have nurtured more than 20 EDA start-ups over the past 10 years.

These EDA start-ups cover the entire SOC and System design spectrum, from system specifications to RTL design, physical design and mask processing, targeting all electronic products: digital, analog, RF, mixed signal, at board- and chip-level. Of course, the EDA market is global, and therefore, most of these EDA start-ups have offices in the USA and in Asia.

Over the years, established EDA vendors have grown their R&D teams in Grenoble and throughout France, as well, both organically and through acquisitions.

Nestled at the foot of the gorgeous mountains of the French Alps in Grenoble, these companies and other members from other French tech hubs, operate within a world-class R&D ecosystem, benefiting from a pool of engineering and PhD talent among the most recognized in the world, the proximity of SoC and system product design activities, silicon R&D (CEA-LETI, SOITEC, ST) and silicon manufacturing (ST). At LETI for instance, joint R&D labs with EDA companies enable immediate access to state-ofthe-art silicon and SoC data, drastically reducing the feedback loop between EDA tools and their application on actual silicon. FD-SOI and RF-SOI are among the key silicon technologies born in Grenoble in recent years.

At DAC 2016, Minalogic is pleased to showcase this bestkept secret: the EDA start-ups which benefit from the unfair advantage of being born in the innovation ecosystem of France and... did I mention they live in the French Alps? ⁽²⁾



ASELTA operates in the IC manufacturing world and provides software solutions for wafer and mask patterning, optimizing the use of e-Beam/multibeam lithography equipment for sub-20nm nodes. Aselta Inscale is a complete, all in one solution, with a unique model based correction technology (on a full e-beam lithography process). It allows better lithography mask quality, increasing wafer yield. It enables next generation lithography related to EUU, ILT, Multibeam... necessary to cope with Moore's law.



ASYGN is a sensor electronics specialist. ASYGN serves the MEMS industry by delivering integrated circuits, lab instruments and software tools for the design, verification and characterization of complete sensor systems.

Recent releases from Asygn include the AS3125 chip for high-performance multi-DOF MEMS IMU, the dBox-Z1 instrument and AS3126 chip for high-frequency resonant sensor characterization, and Tactyle MX for the simulation and verification of Image sensors.



CMP is a Multi-Project Wafer (MPW) service organization in ICs and MEMS for prototyping and low volume production. CMP enables prototypes fabrication on industrial processes at very attractive costs and offers it great technical expertise in providing MPW and related services for Universities, Research Laboratories and Industrial companies' prototyping. Advanced industrial technologies are made available in CMOS, SiGe BiCMOS, HU-CMOS, SOI, MEMS, 3D-IC mostly from STMicroelectronics and ams.



CWS is the leading provider of parasitic extraction and activity modeling tools for system-level interference analysis of complex designs incorporating RF and analog blocks, targeting SOI applications or advanced bulk process nodes. CWS unique harmonic analysis approach allows for controlling and managing noise issues throughout the design cycle from components, to packages, up to and including board design. Wrapped in 'easy-to-deploy' software bundle, WaveIntegrity™ is used by chip architects and designers to drive the chip design floorplanning and by package and PCB designers to integrate the noise-related design constraints in the final chip operational environment.



Defacto Technologies is an innovative chip design software company providing breakthrough RTL platforms to enhance integration, verification and Signoff of IP cores and System on Chips. After more than 10 years of recognized leadership in Design for Test at RTL, Defacto is now offering a complete EDA solution based on generic EDA tools to cover advanced Design Restructuring, Design Verification, Low Power Design, IP Integration & RTL Signoff needs.

Booth 1129

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DEFACTO TECHNOLOGIES

Dolphin Integration contributes to «enabling low-power Systems-on-Chip» for worldwide customers. Over 30 years of experience in the integration of silicon IP components, providing services for ASIC/SoC design and fabrication with its own EDA solutions, make Dolphin Integration a genuine one-stop shop addressing all customers' needs for specific requests. Dolphin Integration is the provider of innovative modeling and simulation EDA solutions.



EdXact is a backend verification specialist, proposing tools for accelerating postlayout analysis flows. Flagship tool is Jivaro, a booster for all simulation tools suffering from the large amount of parasitics. Other tools concern transistor level power grid analysis, powerMOS key parameter extraction and layout comparison. EdXact was founded in 2004 in a suburb of Grenoble, France.

Booth 2019 **ΕΠΧΔΓ.Τ**



Intento-design (2015), operates in the Analog IC EDA market; it proposes an innovative design methodology for shortening the productivity gap inherent to the analog design process. Based on 25 years of research, the Intento solution accelerates the design of analog functions, helping the designer to automate the path from electrical behavior to transistor sizing. It allows fast technology migration and makes analog functions easily reusable.

IROC Technologies provides the semiconductor industry with soft error analysis software, test services, expert advisors and auditing to improve device and system reliability. IROC's EDA tools, TFIT and SOCFIT, are licensed by companies that care about reliability, in application areas such as automotive, avionics, telecommunications and medical devices. IROC's test services provide the semiconductor industry with fast and accurate methods of SER test and analysis for any digital device.

Booth 1638 **IROC TECHNOLOGIES**



Leti is a technology research institute at CEA Tech and a key player worldwide in technologies combining miniaturization, high performance and low power. With a staff of 1,900 and a portfolio of 2,800 patents, Leti partners with global manufacturers, SMEs and startups to tailor innovative solutions that strengthen their competitive positions.

At Leti, Electronic Design Automation (EDA), is covered through common labs with CAD companies. These labs allow CAD companies to evaluate and enhance their tools using Leti advanced circuit and technology test cases.

Follow us: @CEA_Leti.



Magillem is a leading EDA software provider. Internationally renowned, we are present in 12 countries. 90% of our turnover is realized abroad.

Our innovative solution, introducing an XLM-based collaborative platform, supports our customers' R&D from specification of their product to the documentation, and connects all business experts, especially in IoT and embedded systems' domain.



Menta provides programmable logic IPs for your SoC. Menta embedded FPGAs (eFPGA) add flexibility to your products. With Menta solutions, your chips can keep up to date with latest standards or target multiple customers, through RTL re-programming. Menta offers a complete solution: eFPGA IP but also software to size the IP to your specific needs, estimate the performances and generate the eFPGA programs.



Mentor Graphics Corporation is a world leader in electronic hardware and software design solutions, providing products, consulting services and award-winning support for the world's most successful electronic, semiconductor and systems companies. Established in 1981, the company reported revenues in the last fiscal year of approximately \$1.18 billion. Corporate

Booth 949

headquarters are located at 8005 S.W. Boeckman Road, Wilsonville, Oregon 97070-7777.

MENTOR GRAPHICS

Contact marcom_france@mentor.com J-M Saint-Paul, Regional Director Sales, South-West www.mentor.com





MODEMIS



Silvaco, Inc. is a leading EDA provider of software tools used for process and device development and for analog/mixed-signal, power IC and memory design. Silvaco delivers a full TCAD-to-signoff flow for vertical markets including: displays, power electronics, optical devices, radiation and soft error reliability and advanced CMOS process and IP development. For over 30 years, Silvaco has enabled its customers to bring superior products to market at reduced cost and in the shortest time. The company has a French presence in Grenoble.

SILVACO

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TIEMPO SECURE develops and industrializes components for secure communicating devices (banking smartcards, ID documents, IoT connected objects). These components, available as IP cores, include a microcontroller and crypto-processors designed in a proprietary clockless technology, offering therefore a very high level of security against attacks and outstanding performance in speed/energy for contactless operations. TIEMPO also offers a synthesis tool for clockless designs.



The research activities of the TIMA Laboratory focus on the definition of EDA methods and tools for correct and efficient design, simulation, high level synthesis, validation and test of digital integrated components and systems on chip. Its main strengths are fast and accurate simulation and synthesis of hardware/software integrated multiprocessors, correct design at the RT level, and validation and test at the system level.



Shrinking geometries, new manufacturing paradigms, exploding file sizes ... It's time to rethink everything!

XYALIS phases in a new generation of tools redesigned to address the challenges of today's most advanced processes, with a focus on speed and memory usage.

From CMP fill with GOTstyle, to Mask Data Preparation with automated frame generation, MPW placement and mask set edition, and to layout manipulation, XYALIS' redeveloped engines leverage the power of a native OASIS.MASK internal representation.





MINALOGIC



Minalogic is a global innovation cluster for digital technologies serving France's Auvergne-Rhône-Alpes region. The cluster supports the region's leading innovators by facilitating networking, fostering collaborative R&D, and providing companies with personalized assistance throughout all phases of business growth. The products and services developed by our members address all industries, from ICT and healthcare to energy and advanced manufacturing.

Minalogic was founded in 2005 and today boasts more than 300 members, including 270 companies. The cluster has certified nearly 450 projects that have secured total government funding of €794 million of the more than €2 billion in total R&D spending these projects represent. The 56 projects completed to date have resulted in 37 products (either on the market or in the process of being prepared for market release) and generated €1.25 billion in revenue.

- TARGET MARKETS :
- ICT

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- Healthcare
- Energy
- Construction
- Advanced Manufacturing
- Transportation
- Sports & Outdoors





INVEST IN GRENOBLE-ISÈRE FRANCE

AEPI partners with Minalogic, CEA Leti, and others to promote the Grenoble-Alps ecosystem and attract companies to southeastern France. 13

AEPI is based in Grenoble, one of the world's top microelectronics clusters, very well known in the EDA community.

With a North American office in California., AEPI offers businesses exploring options in the area complimentary information, contacts and services that can be provided in confidentiality.

Many US companies active in EDA have operations and/or partnerships in the area. Over the years at DAC, an impressive percentage of exhibitors have been French companies, a majority of which have been Grenoble-based.

COME AND MEET US AT







DAC 2016 Minalogic Showcase: Spotlight on the EDA innovators in France

Tuesday, June 7, from 4-6 p.m. DAC Show floor, SI2 Pavilion, #239 Austin Convention Center

▶ Introduction speech by Philippe Magarshack, President of Minalogic & EVP, STMicroelectronics

Remarks by Guest of Honor, James H. Hogan, managing partner of Vista Ventures, LLC, who will moderate the following panel

Round table and Q&A with following guests:

- Philippe Magarshack, President Minalogic
- Firas Mohamed, General Manager Silvaco France
- Chouki Aktouf, Founder & CEO, DeFacTo Technologies- representative of the EDA SMEs members Minalogic
- Thierry Collette, VP, Architecture, IC Design & Embedded Software Division, Leti

Networking reception

About French EDA

France is renowned as an attractive market and for its talented engineers. The country's research tax credit is the most attractive tax incentive program of its kind in Europe. In a leading "French Tech" region, Minalogic is one of the world's top digital technology clusters. With the Grenoble area's strengths in micro- & nanoelectronics coupled with software capabilities, the ecosystem is well-known in the EDA industry.



For more information : http://www.grenoble-isere.com/dac/

The event is free, but register in advance, raffle/drawing following the panel

Raffle:

noMad BUSINESS (from Dracula Technologies) - noMad Business is a "professional briefcase," a cover to transport AND charge your electronic devices. Ensure an energetic mobility for your tablets and smartphones.

► Hydrao (from <u>Smart & Blue</u>) - The new Hydrao 2.0 is the world first Eco-friendly Smart Showerhead. How much water do you think you used during your last shower?

www.grenoble-isere.com/en www.minalogic.org www-leti.cea.fr/en

AUVERGNE - RhôneAlpes



LIST OF PARTICIPANTS

ASELTA ASYGN CMP (CIRCUITS MULTI-PROJETS) 01 CWS (COUPLING WAVE SOLUTIONS) 02 DEFACTO TECHNOLOGIES 03 DOLPHIN EDXACT 04 INTENTO 05 IROC TECHNOLOGIES 06 LETI-CEA TECH 07













